IN THE SPECIFICATION

Please amend the specification as follows:

Please replace the paragraphs beginning at page 4, line 16, and ending at page 6, line 28, with the following paragraphs:

Summary of the Invention

According to one aspect of the present invention, what is described is a method of executing more than one thread at a time in a computer system having a plurality of threads, including a first and second thread. The method includes providing a first and a second reorder buffer, reading first instructions and first operands associated with the first thread from the first reorder buffer, executing one of the first instructions and storing a result in the first reorder buffer, where storing a result in the first reorder buffer includes marking the result with a tag associating the result with the first thread. The method also includes reading second instructions and second operands associated with the second thread from the second reorder buffer, and executing one of the second instructions and storing a result in the second reorder buffer, where storing a result in a second reorder buffer includes marking the result with a tag associating the result with the second thread.

According to another aspect of the present invention, what is described is a processor comprising an instruction pipeline and a results pipeline that are counter rotating queues, a first execution unit in communication with the pipelines, a plurality of threads including a first and second thread, a first reorder buffer associated with the first thread, a second reorder buffer associated with the second thread, and a first instruction fetch/decode unit.